

What is claimed is:

1. A method for forming an interconnect structure, comprising the steps of:
  - a) providing an insulating layer over a semiconductor structure ;
  - b) forming an opening in said insulating layer;
  - c) forming a fill layer comprised of Cu and Ti over insulating layer;
  - d) in a nitridation step, nitridizing said fill layer to form a self-passivation layer comprised of titanium nitride over said fill layer.
2. The method of claim 1 which further includes after forming said opening:
  - forming a barrier layer over insulating layer;
  - forming a seed layer over said barrier layer; said seed layer comprised of Cu and Ti;
  - and after the step of forming said fill layer; annealing said seed layer and said fill layer to dope said fill layer with Ti from said seed layer.
3. The method of claim 1 wherein in said nitridation step; the nitridation is performed by soaking the semiconductor structure in an  $\text{NH}_3$  ambient at a temperature of between about 150 C and 450 °C and at a pressure of between about 0.2 torr and 760 torr.

4. The method of claim 1 wherein in said nitridation step; the nitridation is performed by soaking the semiconductor structure in an  $N_2/H_2$  ambient at a temperature of between about 150 °C and 450 °C and at a pressure of between about 0.2 torr and 760 torr.
5. The method of claim 1 wherein in said nitridation step; the nitridation is performed by exposing the copper-titanium fill layer to an  $NH_3$  plasma at a temperature of between about 150 °C and 400 °C, at a pressure of between about 0.2 mtorr and 20 mtorr.
6. The method of claim 1 wherein in said nitridation step; the nitridation is performed by exposing the copper-titanium fill layer to an  $N_2/H_2$  plasma at a temperature of between about 150 °C and 400 °C, at a pressure of between about 0.2 mtorr and 20 mtorr.
7. The method of claim 1 wherein said insulating layer is comprised of a low -k material.
8. The method of claim 1 wherein self-passivation layer is comprised of oxygen rich titanium nitride.
9. The method of claim 1 wherein said opening is a dual damascene shaped opening.
10. A method for forming an interconnect structure, comprising the steps of:

- a) forming an insulating layer over a semiconductor structure;  
forming an opening in said insulating layer;
  - b) forming a barrier layer over insulating layer;
  - c) forming a seed layer over said barrier layer;
  - d) forming a copper fill layer over said seed layer ;
  - e) annealing said seed layer and said copper fill layer to form a copper-titanium fill layer;
  - f) in a nitridation step, nitridizing said copper-titanium fill layer to form a self-passivation layer comprised of titanium nitride over said copper-titanium fill layer.
11. The method of claim 10 wherein said opening is a dual damascene shaped opening.
12. The method of claim 10 wherein said insulating layer is comprised of a low -k material.
13. The method of claim 10 wherein said barrier layer comprising TaN.
14. The method of claim 10 wherein said barrier layer is comprised of a material selected from the group consisting of tantalum nitride, molybdenum, tungsten, chromium and vanadium; and has a thickness between 50 and 2000 Å.

15. The method of claim 10 wherein said barrier layer has a thickness between 50 and 2000 Å.
16. The method of claim 10 wherein said seed layer is comprised of copper and titanium.
17. The method of claim 10 wherein said seed layer is comprised of copper and titanium and has a thickness of between about 50 angstroms and 2000 angstroms, said seed layer has a titanium concentration of between about 0.1 and 2.0 weight %.
18. The method of claim 10 wherein said seed layer is comprised of copper and titanium; said seed layer is formed by a sputtering process using a titanium doped copper target; said titanium doped copper target is comprised of between about 0.1 and 2.0 % Ti by weigh.
19. The method of claim 10 wherein said copper fill layer comprised essentially of Cu;
20. The method of claim 10 wherein said copper-titanium fill layer is essentially oxygen free.
21. The method of claim 10 wherein the annealing said seed layer and said copper fill layer is performed at a temperature between about 150 and 450 °C, for a time between about 0.5 and 5 minutes, in an atmosphere of N<sub>2</sub>/H<sub>2</sub> forming gas.

22. The method of claim 10 wherein the Ti from said seed layer comprised of Copper and titanium, is essentially uniformly distributed through the copper –titanium fill layer.

23. A method for forming an interconnect structure, comprising the steps of:

- a) forming an insulating layer over a semiconductor structure;

forming an opening in said insulating layer;

- b) forming a barrier layer over insulating layer;

- c) forming a seed layer over said barrier layer;

- (1) said seed layer is comprised of copper and titanium and has a thickness of between about 50 angstroms and 2000 angstroms, said seed layer has a titanium concentration of between about 0.1 and 2.0 weight %;

- d) forming a copper fill layer over said seed layer; said copper fill layer formed by an electroplating process;

- (1) said copper fill layer comprised essentially of Cu;

- e) planarizing said copper fill layer using a chemical-mechanical polishing process;

- f) annealing said seed layer and said copper fill layer to form a copper-titanium fill layer ;

- (1) said copper-titanium fill layer is essentially oxygen free;

- (2) the annealing said seed layer and said copper fill layer is performed at a temperature between about 150 and 450 °C, for a time between about 0.5 and 5 minutes, in an atmosphere of N<sub>2</sub>/H<sub>2</sub> forming gas;
  - (3) the Ti from said seed layer comprised of copper and titanium, is essentially uniformly distributed through the copper –titanium fill layer;
  - g) in a nitridation step, nitridizing said copper-titanium fill layer to form a self-passivation layer comprised of TiN over said copper-titanium fill layer.
24. The method of claim 23 wherein said insulating layer is comprised of a low -k material.
25. The method of claim 23 wherein said opening is a dual damascene shaped opening.
26. The method of claim 23 wherein said barrier layer comprising TaN.
27. The method of claim 23 wherein said barrier layer has a thickness between 50 and 2000 Å.
28. The method of claim 23 wherein in said nitridation step; the nitridation is performed by soaking the semiconductor structure in an NH<sub>3</sub> ambient at a temperature

of between about 150 °C and 450 °C and at a pressure of between about 0.2 torr and 760 torr.

29. The method of claim 23 wherein in said nitridation step; the nitridation is performed by soaking the semiconductor structure in an  $N_2/H_2$  ambient at a temperature of between about 150 °C and 450 °C and at a pressure of between about 0.2 torr and 760 torr.
30. The method of claim 23 wherein in said nitridation step ; the nitridation is performed by exposing the copper-titanium fill layer to an  $NH_3$  plasma at a temperature of between about 150 °C and 400 °C, at a pressure of between about 0.2 mtorr and 20 mtorr.
31. The method of claim 23 wherein in said nitridation step; the nitridation is performed by exposing the copper-titanium fill layer to an  $N_2/H_2$  plasma at a temperature of between about 150 °C and 400 °C, at a pressure of between about 0.2 mtorr and 20 mtorr.